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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,996	09/19/2005	Joji Fujiwara	MAT-8744US	1009

52473 7590 11/16/2007

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EXAMINER	
CRAWFORD, LATANYA N	
ART UNIT	**PAPER NUMBER**
2813	

MAIL DATE	DELIVERY MODE
11/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/549,996	FUJIWARA ET AL.	
	Examiner	Art Unit	
	LaTanya Crawford	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/19/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/19/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action, for application no. 10/549,996, is in response to the amendment filed on August 27, 2007.

Status of Application

2. Claims 1-22 are pending in this application. If the applicant is aware of any prior art or any other co-pending application not already of record, he/she is reminded of his/her duty under 37 CFR 1.56 to disclose the same.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this Office action:

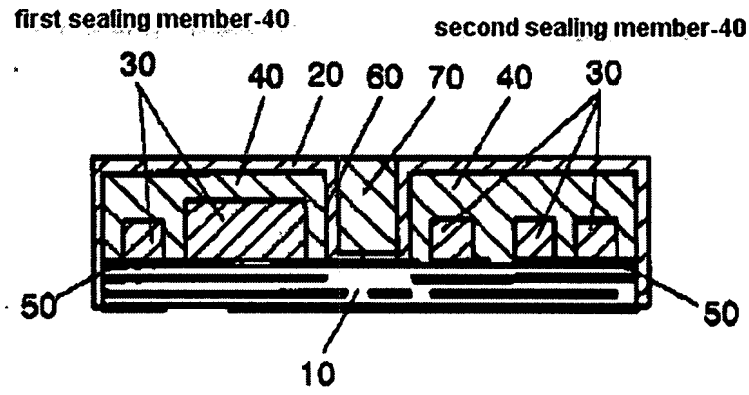
> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-3,5,8-10,13,15-18, &20-22** are rejected under 35 U.S.C. 102*(e)* as being anticipated by **Tsuneoka (US Pub no. 2004/0252475 A1).**

Regarding claim 1, Tsuneoka et al. discloses a module component comprising: a substrate **10** a partition **70** formed on the substrate **10 (fig. 5)**, the partition **70** having a predetermined height to divide the substrate **10** into a plurality of circuit blocks **(fig. 5; [0023], lines 14-16; [0025], lines 1-3)**; a first sealing member **40 (first portion of element 40, on the left in fig. 5)** covering the plurality of circuit blocks; a second

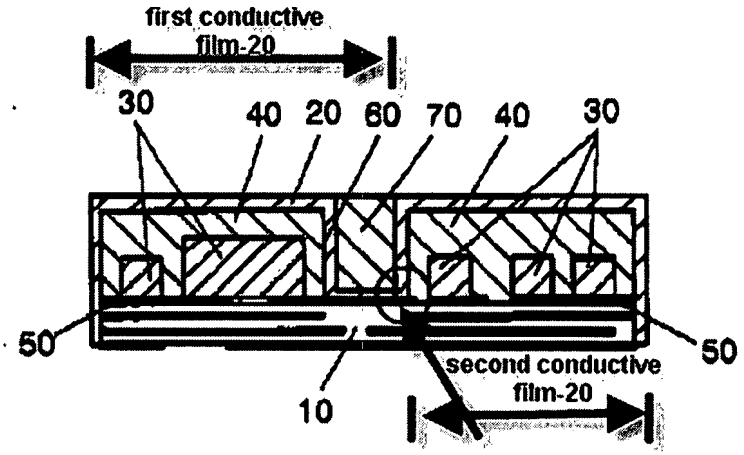
sealing member **40 (second portion of element 40, on the right in fig, 5)** covering a second circuit block of the plurality of circuit blocks;

FIG. 5



a first conductive film **20 (first portion of element 20, on the left in fig. 5)** covering at least a surface of the first sealing member **40 (first portion of element 40, on the left of in fig, 5)** and a second conductive film **20 (second portion of element 20, on the right in fig. 5)** covering at least a surface of the second sealing member; wherein the plurality of circuit blocks are electrically shielded individually **([0026], lines 4-7)**.

FIG. 5



Regarding claim 2, Tsuneoka et al. teaches the partition **70 (view fig. 5; [0025], lines 1-3; [0026] lines 1-3)** is made of resin and conductive material **(view fig. 5; [0028], lines 1-9)**; and the first sealing member **40 (first portion of element 40, on the left of in fig, 5)** , the second sealing member **40 (second portion of element 40, on the right in fig, 5)** and the partition **70** contain a same resin **(view fig. 5; [0028], lines 1-9).**

Regarding claim 3, Tsuneoka et al. teaches the partition **70 (view fig. 5; [0025], lines 1-3; [0026] lines 1-3)** is made of ceramic powder-containing resin and conductive material **20 (view fig. 5; [0028], lines 1-9)**; and the first sealing member **40 (first portion of element 40, on the left of in fig, 5),** the second sealing member **40 (second portion of element 40, on the right in fig, 5)** and the partition **70** contain a same resin **(view fig. 5; [0028], lines 1-9).**

Regarding Claim 5, Tsuneoka et al. teaches the conductive material of the partition **70** is a conductive resin **([0028], lines 1-9)**.

Regarding claim 8, Tsuneoka et al. teaches the partition **70** has a conductive wall **20** in a direction vertical to the substrate **10 (view fig. 5)**.

Regarding claim 9, Tsuneoka et al. teaches the partition is formed by stacking at least one metal film **20** and ,resin **70**; and the metal film is formed to be parallel with the longitudinal direction of the partition **70** and to be vertical to the substrate **10 (fig 5)**.

Regarding claim 10, Tsuneoka et al. teaches the partition **70** has resin at least one side surface thereof **(view fig. 5)**.

Regarding claim 13, Tsuneoka et al. teaches the partition **70** has a planar shape of a letter T **(fig. 4).**

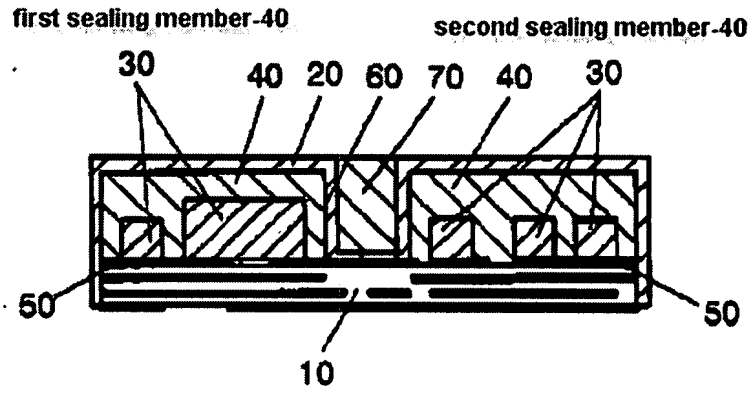
Regarding Claim 15,Tsuneoka et al. discloses the partition **70** is higher than an electric component mounted **30** on the substrate **10 (view fig. 5).**

Regarding claim 16, Tsuneoka et al. teaches the substrate **10** has a ground pattern **50** on a surface thereof, and the ground pattern **50** is connected with the first conductive film **20 (first portion of element 20, on the left in fig. 5)** and second conductive film **20 (second portion of element 20, on the right in fig. 5) ([0018] lines 15-17).**

Regarding claim 17, Tsuneoka et al. discloses a method for manufacturing a module component having a plurality of circuit blocks shielded individually, the method comprising: a step of mounting a partition **70** higher than mounting components **30 (fig.5)**, the partition **70** dividing mounting components and a substrate **10** into a plurality of circuit blocks on the substrate **10**; a step of forming a first sealing member **40 (first portion of element 40, on the left in fig. 5)** covering a first circuit block of the plurality of circuit blocks individually in such a manner as to be higher than the mounting components **30** ; a step of forming a second sealing member **40 (second portion of**

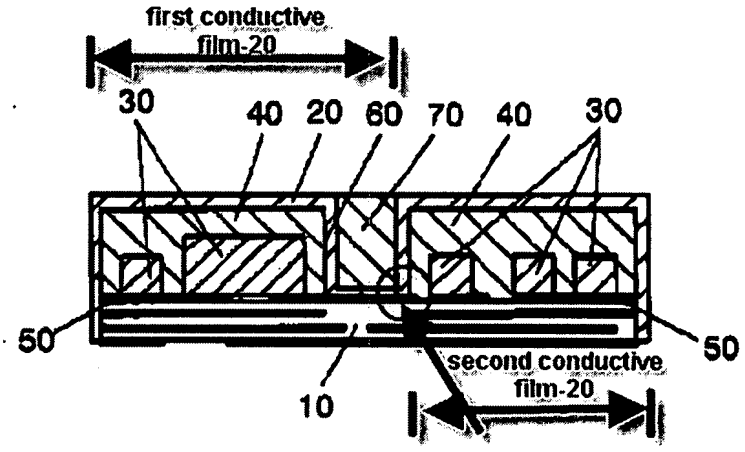
element 40, on the right in fig. 5) covering a second circuit block of the plurality of circuit blocks individually in such a manner as to be higher than the mounting components **30**;

FIG. 5



a step of forming a first conductive film **20 (first portion of element 20, on the left in fig. 5)** on a surface of the first sealing member **40 (first portion of element 40, on the left in fig. 5)** and a step of forming a second conductive film **20 (second portion of element 20, on the right in fig. 5)** on a surface of the second sealing member**40 (second portion of element 40, on the right in fig. 5)**.

FIG. 5



Regarding claim 18, Tsuneoka et al. discloses the partition **70** contains a conductive material **([0028], lines 1-9)** formed in a direction vertical to the substrate **10 (fig. 5)**; and the step of forming a first sealing member **40 (first portion of element 40, left region in fig. 5).**

Regarding claim 20, Tsuneoka et al. discloses the step of forming a first conductive film **20 (first portion of element 20, on the left in fig. 5)** or the step of forming a second conductive film includes a step of connecting the respective conductive film **20 (second portion of element 20, on the right in fig. 5)** with a ground pattern **50 (fig. 5; 0026], lines 4-6).**

Regarding claim 21, Tsuneoka et al. discloses wherein the first and second conductive films 20 (first and second portion of element 20, on the left in fig. 5) are separated by the partition 70 (fig. 4 & 5; [0023],lines1-3).

Regarding claim 22, Tsuneoka et al. discloses wherein the partition **70 [0028]** electrically connects the first conductive film **20 (first portion of element 20, on the left in fig. 5)** with the second conductive film **20 (second portion of element 20, on the right in fig. 5) (view. Fig. 5).**

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuneoka (US Pub no. 2004/0252475 A1)** in view of **Warren (US Pub no. 2002/0126018 A1).**

Regarding claim 4, Tsuneoka et al. discloses all of the claimed limitations from above but fails to teach the partition is a metal foil.

However, Warren et al. teaches the partition **210** is a metal foil **([0032] lines 1-3).** It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with a shielding partition constructed of metal foil taught by Warren et al. Doing so would provide improved performance and reduction of coupling between electronic components.

7. **Claims 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuneoka (US 2004/0252475 A1)** in view of **Oda (US 2002/0051340).**

Regarding Claim 6, Tsuneoka et al. discloses all of the claimed limitations from and further teaches the partition **70** is resin having a metal film **20** formed on an outer surface thereof **(fig. 5)** but fails to teach the partition is resin having a metal film formed on an outer surface thereof, and has a square cross section in a longitudinal direction.

However Oda et al. teaches the partition **94A** having a square cross-section in a longitudinal direction **(fig 9; [0048], lines 1-2)**. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the module component of Tsuneoka et al. with a partition having a square cross section taught by Oda et al. since doing so would provide improved efficiency of the module.

8. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuneoka (US Pub no. 2004/0252475 A1)** in view of **Witty (US Patent 6,380,491 B1).**

Regarding claim 7, Tsuneoka et al. discloses all the claim language from above and further teaches the partition **70** is resin having a metal film **20** formed on an outer surface thereof **(fig. 5)** but fails to teach has a cross section with a protruding base in a longitudinal direction.

However, Witty et al. teaches a partition **102** having a cross section with a protruding base in a longitudinal direction **(column 3, lines 1-3).** It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with a partition having a protruding base taught by Witty et al. Doing so would provide improved shield efficiency.

9. **Claim 11 &12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuneoka (US Pub no. 2004/0252475 A1)** in view of **Learmonth (US Patent 6,049,468).**

Regarding claim 11, Tsuneoka et al. discloses all the claim language from above but fails to teach the partition is positioned inside the substrate, and has a planar shape of one of a circle and a polygon.

However, Learmonth et al. discloses the partition **50** is positioned inside the substrate **14**, and has a planar shape of one of a circle and a polygon **(fig. 4)**. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with a partition position inside the substrate having a planar shape of a polygon taught by Learmonth et al. Doing so would

permit the partition to act as a spacer to maintain constant thickness of a PC card and thereby resist flexing of the PC card without damage to the circuit board.

Regarding claim 12, Tsuneoka et al. invention as modified by Witty et al. discloses all the claim language from above but fails to teach the partition is positioned out of contact with an outer edge of the substrate.

However, Learmonth et al. discloses the partition **50** is positioned out of contact with an outer edge of the substrate **14 (fig. 4).** It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with a partition position inside the substrate having a planar shape of a polygon taught by Learmonth et al. Doing so would permit the partition to act as a spacer to maintain constant thickness of a PC card and thereby resist flexing of the PC card without damage to the circuit board.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuneoka (US Pub no. 2004/0252475 A1)** in view of **Weekamp (US Pub no. 2007/0052091 A1).**

Regarding claim 14, Tsoneoka et al. invention discloses all of the claimed limitations of claim 1 above but fails to teach the first conductive film and the second conductive film include metal and conductive resin.

However, Weekamp et al. teaches the conductive film include metal ***foil*-40** and conductive resin **42, 43 (fig. 2; [0056], lines 3-5;[0053], lines 6-8)**, It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with a conductive film including foil and

conductive adhesive taught by Weekamp et al. since doing so would provide electrical contact.

11. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuneoka (US Pub no. 2004/0252475 A1)** in view of **Percival (US Patent 4,691,434).**

Regarding claim 19, Tsuneoka et al. discloses all of the claimed limitations from claim 17 above but fails to teach a step of removing the conductive material by one of dicing and laser.

However, Percival et al. teaches a step of removing the conductive material by one of dicing and laser **(Abstract, lines 8-14).** It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the module component of Tsuneoka et al. with removing the conductive material by laser taught by Percival et al. since doing so provides connections to underlying electronic components.

Response to Arguments

12. Applicant's arguments with respect to claim 1-22 have been considered but are moot in view of the new ground(s) of rejection. To further explain the examiner's position with regards to amended claims 1 & 17, Tsuneoka et al. discloses several embodiments, in view of **fig. 4 [0023], lines 1-3**, the sealing body **40** covered with the metal film **20** is **divided** into three blocks by means of a sealing body ***(partition)* 70**. Hence, if the sealing body is divide into three blocks, the metal film is also divided providing a plurality of conductive films. Also in view of fig. 5, two metal films are disclosed as indicated in the figure imported, where referenced in this action.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaTanya Crawford whose telephone number is (571) 270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM -5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LaTanya Crawford

November 9, 2007

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